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JUN 04 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor : Ruitenburg
Application No. : 10/516,548
Filed : 12/02/2004
For : RECEIVER SIGNAL STRENGTH INDICATION

APPEAL BRIEF

On Appeal from Group Art Unit 2618


Date: 06/04/2007

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Michael Ure
(Name)

 6/4/07
(Signature and Date)

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RELATED PROCEEDINGS

EVIDENCE

TABLE OF CASES

NONE

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I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1, 3 and 4 are pending, all of which stand finally rejected and form the subject matter of the present appeal. Claim 2 has been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a received signal strength indication that may be used, for example, in a cable modem or the like. As illustrated in the Figure, the amplification chain includes a series of discretely-controlled amplifiers, a discretely-

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controlled filter SF1, a mixer M, a fixed filter SF2, and a final continuously-controlled amplifier. The signal strength of the input signal must be accurately detected and reported back, for example to the head-end of a cable system. The RSSI circuit includes a narrow-band filter NF, and logarithmic detector (log) and an analog-to-digital converter (ADC). This combination of elements is recited in independent claim 1.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A receiver signal strength indication circuit receiving a discretely controlled amplified signal from an amplifying means (A1-A4), the circuit comprising:	Figure, RSSI, A1-A4	Page 1, line 18 to page 2, 8; page 3, lines 17-32.
narrow filter means coupled to an output of the discretely controlled amplifying means (A1-A4), said narrow filter means providing a limited spectrum of the input signal;	Figure, NF	Page 4, lines 1-15.
logarithmic detector means for receiving and logarithmically amplifying an output of the narrow filter; and	Figure, log	Page 3, lines 3-5.
ACD means for converting the output of the logarithmic detector to a digital receiver signal strength indication.	Figure, ADC	Page 2, lines 1-8.

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VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 103(a), claims 1, 3 and 4 are unpatentable over Lampe in view of Yano and Toshida.

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Toshida

The combination of references set forth in the final rejection is unfounded.

Lampe relates to a cellphone handset receiver that uses an active bandpass filter in lieu of a more expensive ceramic filter. Automatic gain control is used to extend the dynamic range of the active bandpass filter. Reconstruction of an RSSI signal is performed to make the RSSI measurement independent of the varying gain.

Yano relates to a dual-mode digital/analog cellphone handset receiver. Filtering is performed in such a way that, for purposes of RSSI measurements, a first filter is used to avoid measurement of adjacent channel signal energy, and for purposes of digital reception, a second filter is used to improve bit error rate. An automatic gain control circuit 30 is used on the digital signal path.

Toshida relates to an analytic instrument (i.e., spectrum analyzer) incorporating a cellphone handset receiver.

It would not have been obvious to combine the teachings of Lampe and Yano in the manner suggested. In the first instance, the receiver architectures of Lampe and Yano are totally different. Lampe relates to a "zero-IF" receiver in which no heterodyning (frequency down-conversion) is performed. Yano, on the other hand, relates to a double (or triple) -heterodyne architecture. More importantly, the elements of Yano proposed to be combined in the RSSI circuit of Lampe are not used in Yano for RSSI. Rather, they are used for automatic gain control (AGC). There is nothing in the reference that would

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teach or suggest incorporating elements of the AGC circuit of Yano into the RSSI circuit of Lampe.

The further combination of Toshiba does nothing to cure the underlying deficiency of the rejection.

With regard to dependent claims 3 and 4, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.


In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

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VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

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IX. APPENDIX: THE CLAIMS ON APPEAL

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1. A receiver signal strength indication circuit receiving a discretely controlled amplified signal from an amplifying means (A1-A4), the circuit comprising:

narrow filter means coupled to an output of the discretely controlled amplifying means (A1-A4), said narrow filter means providing a limited spectrum of the input signal;

logarithmic detection means for receiving and logarithmically amplifying an output of the narrow filter; and

ACD means for converting the output of the logarithmic detector to a digital receiver signal strength indication.

3. An integrated tuner comprising a receiver signal strength indication circuit as claimed in claim 1, wherein the amplifying means (A1-A4, SF1, SF2, M) include selectivity filtering means (SF1, SF2).

4. An integrated tuner comprising a receiver signal strength indication circuit as claimed in claim 1, wherein the amplifying means (A1-A4, SF1, SF2,) include a mixer (M).

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X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE